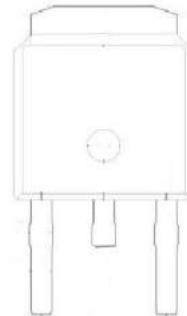
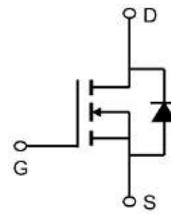


40V N-Channel Enhancement Mode MOSFET
Description

The 80N04D uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.


General Features

$V_{DS} = 40V$ $I_D = 80A$

$R_{DS(ON)} < 7.5m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply


Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

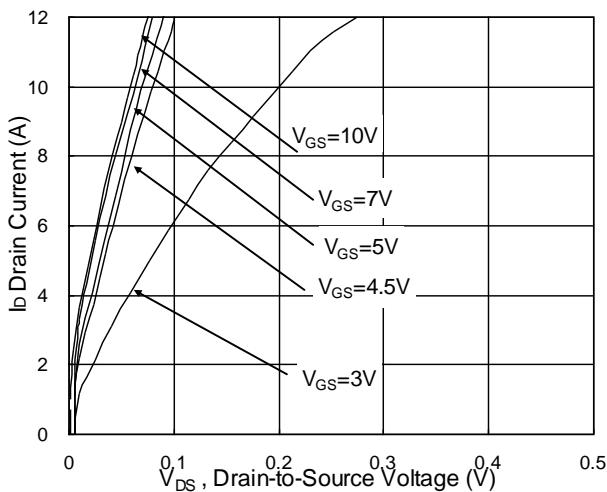
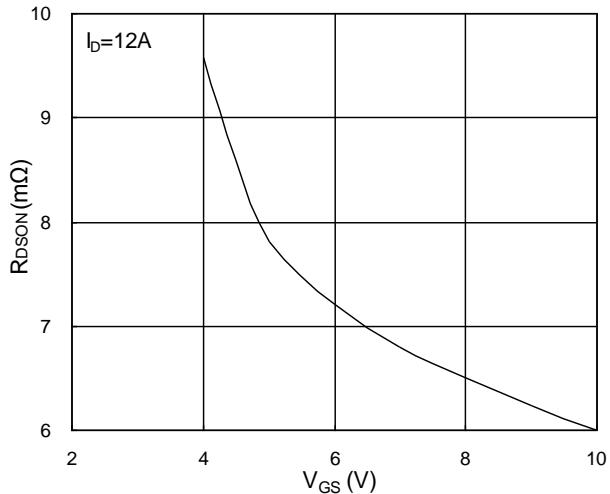
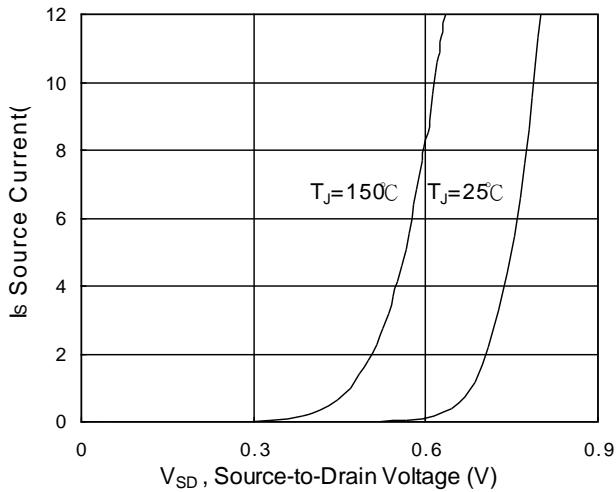
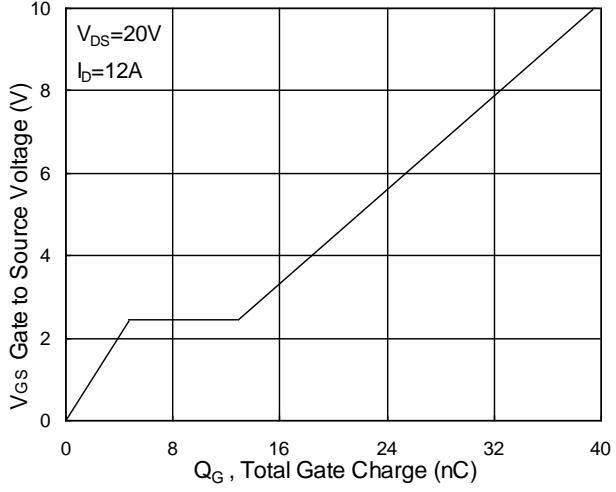
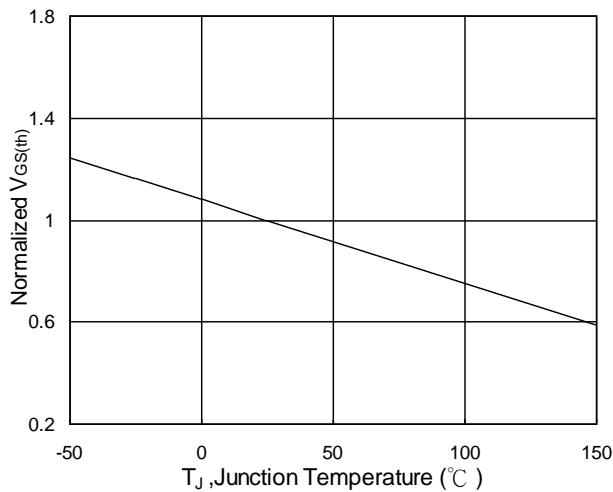
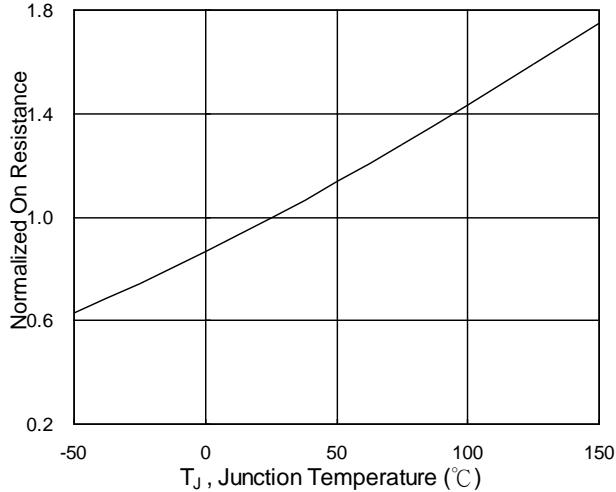
Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	80	A
$I_D@T_c=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	45	A
I_{DM}	Pulsed Drain Current ²	120	A
EAS	Single Pulse Avalanche Energy ³	76.1	mJ
IAS	Avalanche Current	39	A
$P_D@T_c=25^\circ C$	Total Power Dissipation ⁴	44.6	W
TSTG	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
R_{eJA}	Thermal Resistance Junction-ambient (Steady State) ¹	62	°C/W
R_{eJC}	Thermal Resistance Junction-Case ¹	2.8	°C/W

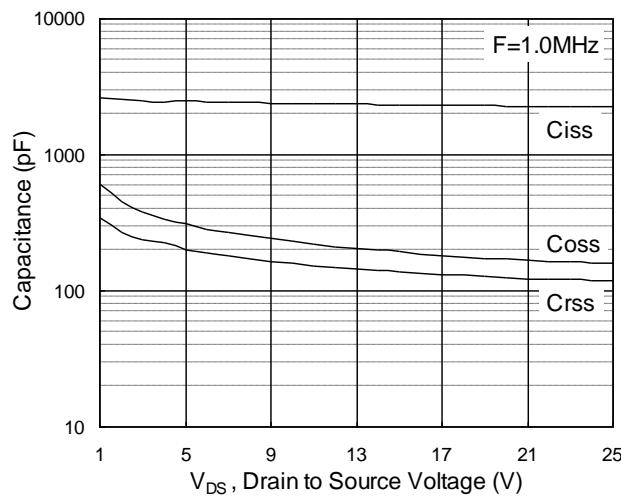
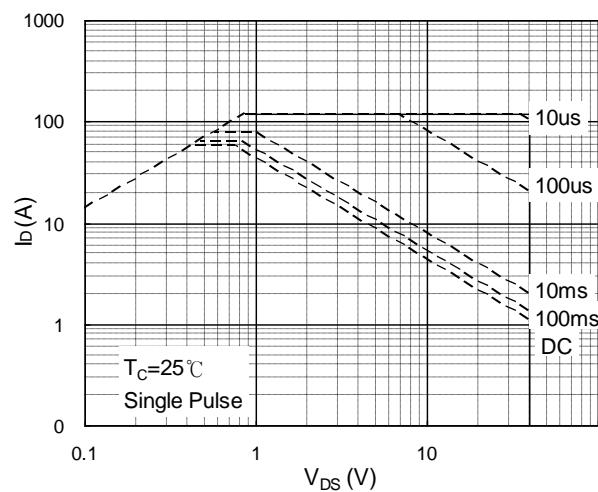
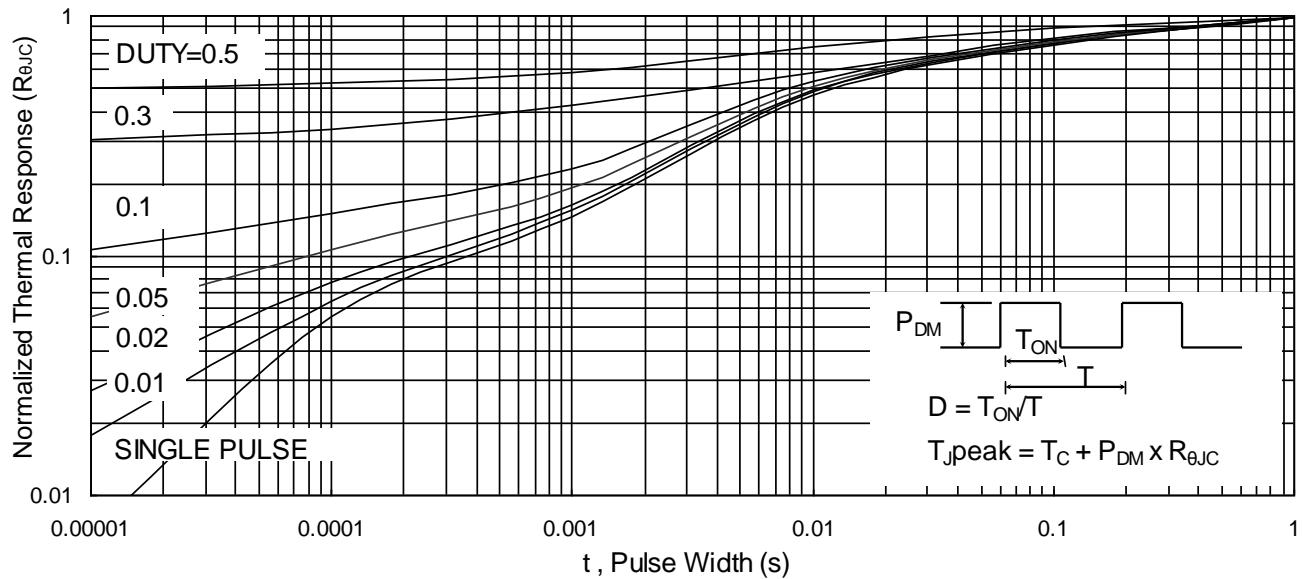
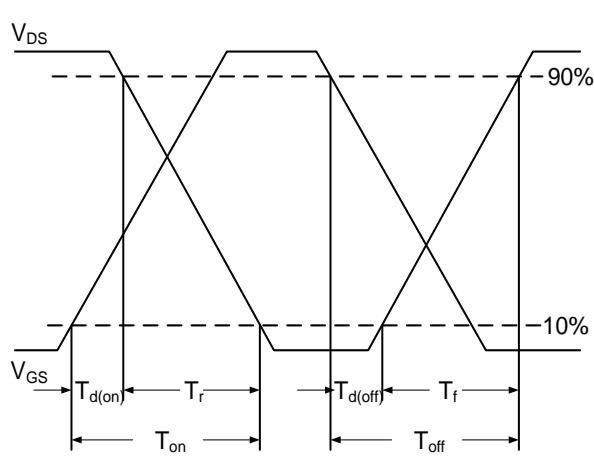
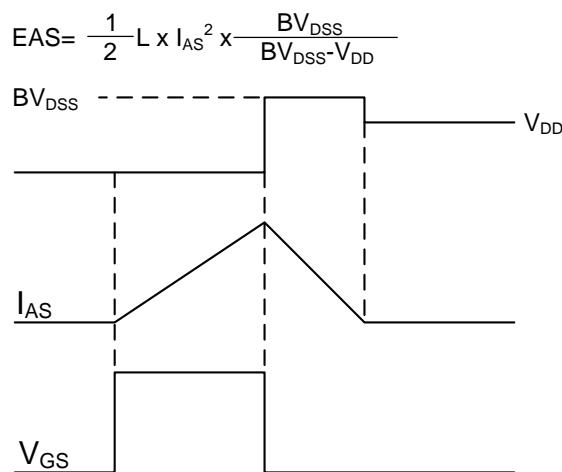
40V N-Channel Enhancement Mode MOSFET
Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

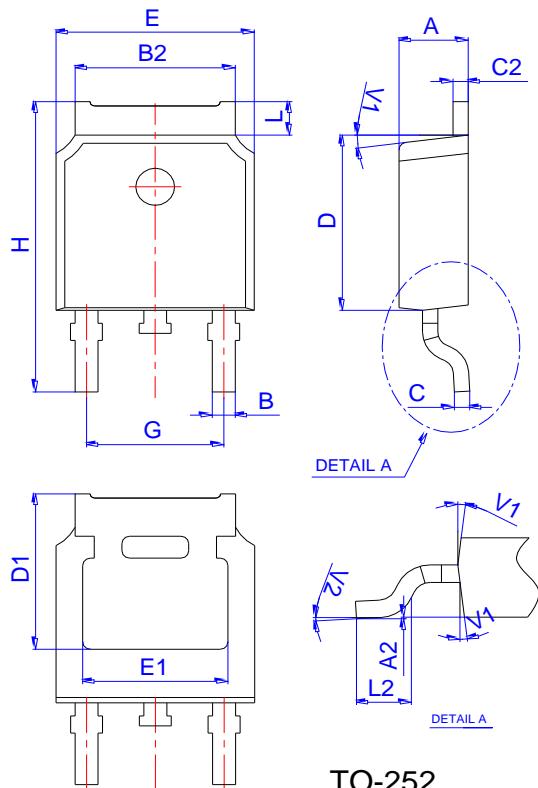
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	40	47	---	V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.034	---	$\text{V}/^\circ\text{C}$
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=10\text{V}$, $I_D=12\text{A}$	---	6.0	7.5	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=10\text{A}$	---	9.0	12	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	1.0	1.5	2.5	V
$\Delta V_{GS(\text{th})}$	$V_{GS(\text{th})}$ Temperature Coefficient		---	-4.96	---	$\text{mV}/^\circ\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=32\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{DS}=32\text{V}$, $V_{GS}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=12\text{A}$	---	39	---	S
R _g	Gate Resistance	$V_{DS}=0\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	1.6	---	Ω
Q _g	Total Gate Charge (4.5V)	$V_{DS}=20\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=12\text{A}$	---	18.8	---	nC
Qgs	Gate-Source Charge		---	4.7	---	
Qgd	Gate-Drain Charge		---	8.2	---	
Td(on)	Turn-On Delay Time	$V_{DD}=15\text{V}$, $V_{GS}=10\text{V}$, $R_G=3.3\text{k}\Omega$ $I_D=1\text{A}$	---	14.3	---	ns
T _r	Rise Time		---	2.6	---	
Td(off)	Turn-Off Delay Time		---	77	---	
T _f	Fall Time		---	4.8	---	
Ciss	Input Capacitance	$V_{DS}=15\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	2332	---	pF
Coss	Output Capacitance		---	193	---	
Crss	Reverse Transfer Capacitance		---	138	---	
IS	Continuous Source Current ^{1,5}	$V_G=V_D=0\text{V}$, Force Current	---	---	60	A
ISM	Pulsed Source Current ^{2,5}		---	---	120	A
VSD	Diode Forward Voltage ²	$V_{GS}=0\text{V}$, $I_S=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1	V

Note :

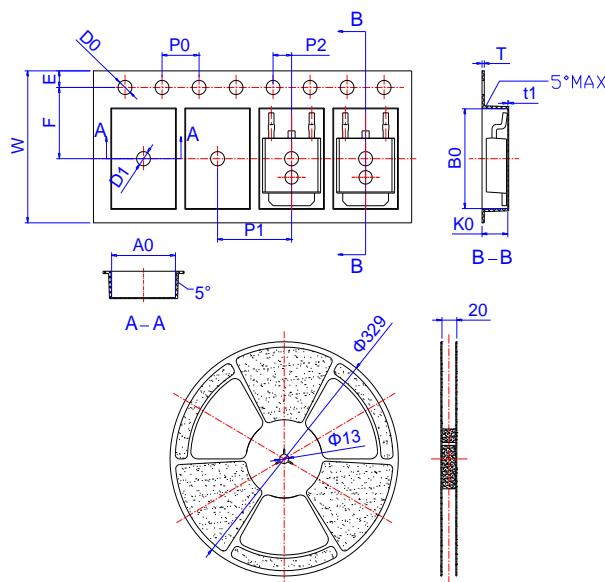
- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $VDD=25\text{V}$, $VGS=10\text{V}$, $L=0.1\text{mH}$, $IAS=39\text{A}$
- 4 .The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

40V N-Channel Enhancement Mode MOSFET
Typical Characteristics

Fig.1 Typical Output Characteristics

Fig.2 On-Resistance vs. G-S Voltage

Fig.3 Forward Characteristics of Reverse

Fig.4 Gate-Charge Characteristics

Fig.5 Normalized $V_{GS(th)}$ vs. T_J

Fig.6 Normalized $R_{DS(on)}$ vs. T_J

40V N-Channel Enhancement Mode MOSFET

Fig.7 Capacitance

Fig.8 Safe Operating Area

Fig.9 Normalized Maximum Transient Thermal Impedance

Fig.10 Switching Time Waveform

Fig.11 Unclamped Inductive Waveform

Package Mechanical Data: TO-252-3L

TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252


Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583